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Abstract

The advancement of high-frequency applications, especially for 5G technology, demands PCBs endure thermal shock during soldering while preserving signal integrity. Traditional copper foil surface treatments to improve resin adhesion increase signal loss due to surface roughening. As the industry adopts foils with extremely low surface profiles for improved signal integrity, methods are needed to correlate foil surface properties with signal integrity, and new methods of assessing the foil-to-low-loss dielectric bond are required. This iNEMI-organized project is addressing these challenges.

Scope of Work

The paper presents data obtained using non-contact profilometry methods, including the Developed Interfacial Area Ratio, Sdr, and preliminary data from a Ruby Dielectric Resonator, measuring the effective conductivity of copper foils. These measurements are then correlated to microstrip insertion loss measurements on 12 sets of foil and oxide alternative treated surfaces. Two electrodeposited and one rolled-annealed copper foil grades, each with two roughness levels are included. Measurements are included of the foil surface bonded to laminate dielectric as well as the top side, treated with different levels of oxide alternative treatment.

The combination of extremely low-profile foils with low-loss dielectrics also raises concerns with thermomechanical reliability and bond-line conductive anodic filament (CAF) growth. The study will include a preliminary assessment of methods that might be used to evaluate these properties on laminates for new test method development. These findings may provide a foundation for a subsequent project.

This iNEMI project aligns with its PCB Roadmap and builds upon prior work performed by the HDP Users Group

Introduction

This project is organized around three main tasks:

- Copper Foil Surface Metrology: contact profilometry has been the historical method used to characterize surface roughness of copper foils. However, as the industry adopts lower and lower levels of roughness to improve signal integrity performance, contact profilometry no longer provides accurate measurement of the surface, and non-contact methods are required, as illustrated in Figure 1. An advantage of non-contact measurement systems is the ability to measure an area of a surface vs. individual points or lines, enabling calculation of additional roughness parameters including the Developed Interfacial Area Ratio, Sdr, which compares the measured surface area in comparison to a planar surface of the same x-y dimension. However, one concern with non-contact methods is the consistency of measurements across differing non-contact measurement systems. An alternative approach to characterizing the copper foil surface is measurement of surface conductivity. Data collected by use of a Ruby Dielectric Resonator is presented and correlated to signal integrity measurements.

- **Signal Integrity:** microstrip test vehicles were manufactured using 12 sets of copper foil and oxide alternative treated surfaces. When electrodeposited (ED) copper foil is manufactured, there is a “drum side” and a “solution side”. The drum side is the surface of the foil in contact with a rotating drum upon which copper is electroplated. The solution side is the surface in contact with the copper sulfate containing solution from which the copper is plated. Since either side can be placed against the dielectric of a copper clad laminate (CCL), to avoid confusion we will use the terms “top side” and “bottom side” where top side refers to the visible, external surface of a copper clad laminate and bottom side refers to the surface bonded to the dielectric of the laminate. Rolled-Annealed (RA) copper foil is produced with a different process, but we will adopt the same ‘bottom’ and ‘top’ terminology when referring to sides typically bonded to the dielectric in a CCL vs. the external side. Standard microstrip testing will be affected mainly by the bottom side of the copper foil. However, in multilayer printed circuit boards (PCBs), the top side is typically surface treated to improve adhesion of this surface to the dielectric used to bond the layers together. To assess the impact of this surface treatment, usually referred to as the “oxide alternative” treatment, we also intentionally manufactured CCLs with the surface treated ‘top side’ against the dielectric in the CCL for this microstrip testing.
- **Reliability:** as the surface roughness is reduced to improve signal integrity, it becomes more challenging to ensure adequate bond strength of the copper foil to the polymers used in the dielectric materials. Our industry historically relied on copper peel strength methods to assess this bond strength. But some copper foil grades increasingly being used in commercial applications for signal integrity benefits cannot meet existing industry standards for peel strength, especially when combined with new extremely low loss dielectric materials. Even so, many of these copper foil grades, though not all, have proven to be reliable in multilayer PCBs. The challenge we face is that traditional peel strength test methods have not been shown to adequately predict reliability in multilayer PCBs. The scope of the current project includes only a preliminary assessment of test methods defined in existing industry standards as well as potential modified test methods. Results from the current project may provide the basis for subsequent study.

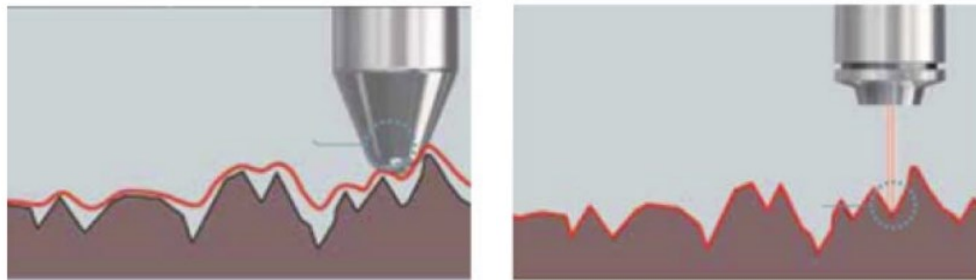


Figure 1 – Contact Profilometry (Left) vs. Non-Contact Profilometry (Right)

Materials & Processes

Two suppliers of ED copper foil provided test samples, and a flexible CCL supplier provided samples of RA copper foil. All copper foils are 1/2-ounce samples. Each supplier provided samples with two levels of surface roughness. For the oxide alternative surface treatment, one supplier provided samples from three different oxide alternative processes for roughness measurements, with the two lower roughness processes used for the microstrip and surface conductivity measurements, which were used only on each foil supplier’s lower roughness grade of copper foil. All CCL samples were manufactured using one supplier’s extremely low loss dielectric material.

Table 1 – Copper & Oxide Alternative Process Variables

Variables		Levels		
A	Copper Type	Electrodeposited (ED - 2 Suppliers)	Rolled Annealed (RA - 1 Supplier)	
B	Foil Roughness	"Low"	"High"	
C	Oxide Alternative	A - Lowest Roughness	B - Low Roughness	C -Standard Roughness

In the manufacturing of printed circuit boards (PCBs), the copper foil undergoes two primary treatments. The first treatment is applied by the copper foil supplier during the foil production process. This treatment is applied to the side of the foil that will be pressed against the dielectric of a CCL (bottom side). The second treatment is carried out by the PCB fabricator during the multi-layer manufacturing process. This treatment employs oxide alternatives (OAs) to enhance the adhesion between the etched circuit pattern and the resin in the prepreg or film used to bond layers of the PCB together (on the top side and edges of the circuit pattern). Given that the surface topology differs between the top and bottom sides of the copper foil, both sides must be carefully considered in the overall manufacturing process.

The influence of the oxide alternative (OA) treated side on loss becomes particularly significant when utilizing stripline technology. In this configuration, current flows along both sides of the copper foil and its edge walls, resulting in copper loss equally attributed to the surface topology of both sides. To isolate the effects of the OA treatment from the bottom side, while also expediting the process and reducing costs, microstrip trace technology is employed. In this transmission line design, surface current is primarily concentrated beneath the trace surface and the ground side laminated against the substrate, which minimizes the contribution from the side opposite the ground plane.

To facilitate this comparison, two types of laminates are prepared. The first laminate features the bottom side laminated against the substrate material as in standard CCLs. The second laminate has the top side, treated with an OA, pressed against the substrate material in a manner similar to the bottom side. Figure 2 illustrates a representative image of the two copper foils and their respective treatment sides.

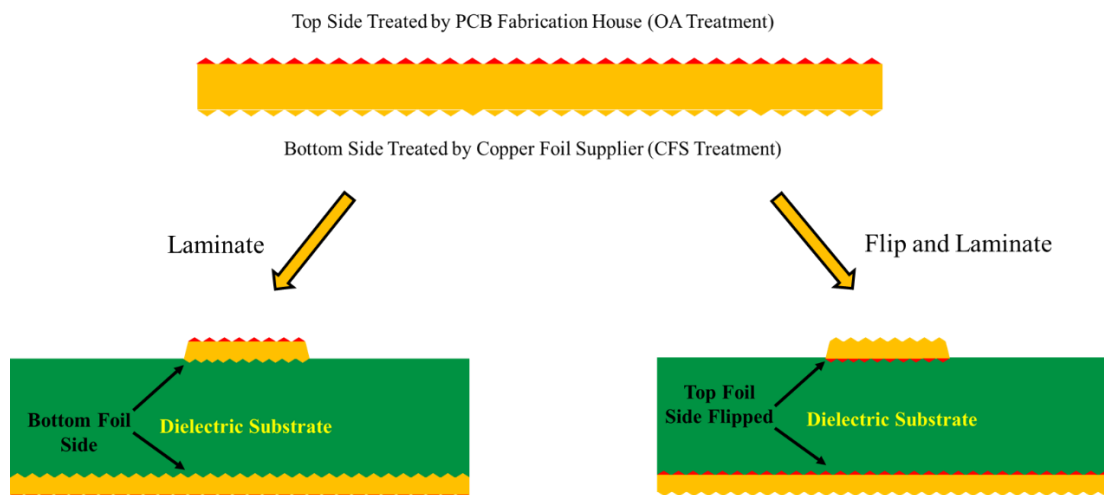


Figure 2 - Foil Treatment Sides for Microstrip Testing

The Design of Experiments (DOE) incorporates six types of copper foil sourced from three different suppliers. Each supplier provided both high-profile and low-profile copper foils. For the high-profile copper, only the effects of the bottom side are considered, while both sides of the low-profile copper foils are evaluated. Samples of the low-profile foils also underwent treatment with two types of oxide alternatives (OAs): Type A, which produces a smoother surface, and Type B, designed to create higher surface roughness. The experimental matrix for the DOE is detailed in Table 2, encompassing a total of twelve distinct cases.

Table 2 – Copper Foils used for Microstrip Test Vehicles

Sample Label	Copper Type	Surface Profile	OA Treatment	Treated Side
H1	ED	High	-	Bottom
L1	ED	Low	-	Bottom
H2	ED	High	-	Bottom
L2	ED	Low	-	Bottom
H3	RA	High	-	Bottom
L3	RA	Low	-	Bottom
L1-A	ED	Low	A	Top
L1-B	ED	Low	B	Top
L2-A	ED	Low	A	Top
L2-B	ED	Low	B	Top
L3-A	RA	Low	A	Top
L3-B	RA	Low	B	Top

Eighteen sheets were allocated for each type of copper for construction of microstrip coupons, measurement of surface resistivity, and assessment of surface topology parameters. Table 3 outlines the required size and quantity of sheets needed for each testing method.

Table 3 – Copper Sheets for Each Copper Type

Test Type	Microstrip Coupons	Effective Conductivity RuDR 28GHz/44GHz	Roughness Measurements
Number of Sheets	10	2	2
Foil Size	22in × 26in	22in × 26in	22in × 26in
Weight	½ oz	½ oz	½ oz
Sample Size	1in and 12.5in	0.787in × 1.18in	2inx1in

The process flow is illustrated in Figure 3.

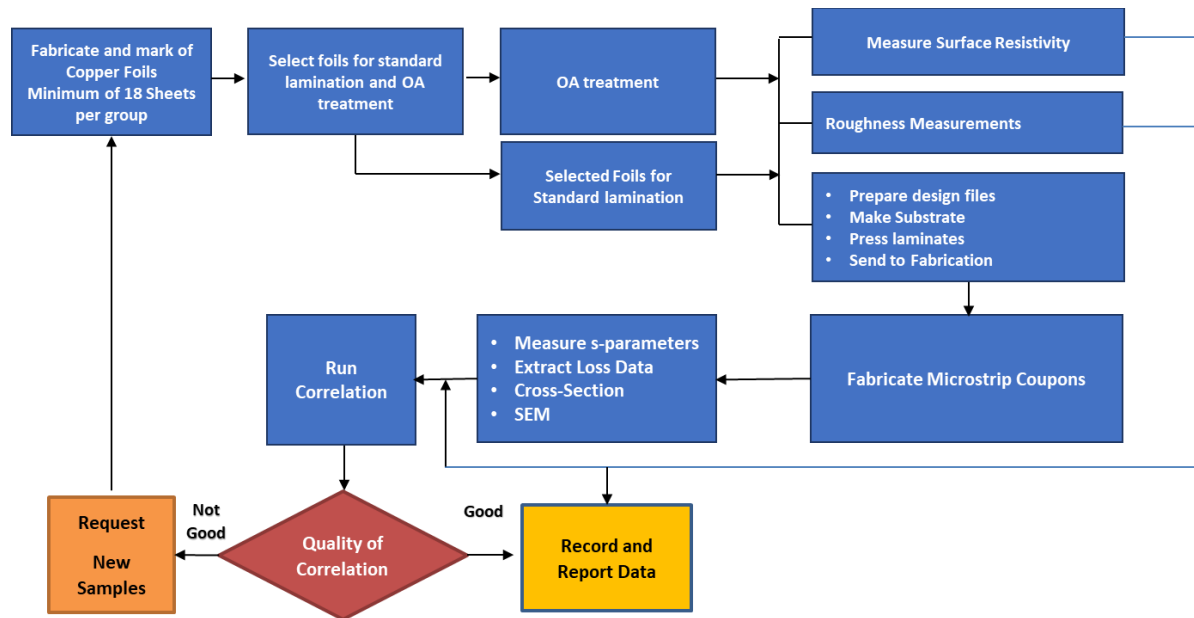


Figure 3 - DOE Process Flow

Microstrip Test Specimens

The signal integrity coupons developed for the Design of Experiments (DOE) utilize microstrip transmission line technology, which is etched onto a two-layer board. This microstrip approach offers several advantages, including reduced fabrication turnaround time, cost-effectiveness, ease of preparation, and straightforward testing. For the substrate material we selected a single supplier's extremely low-loss and halogen-free material. Figure 4 illustrates the design parameters utilized for the test coupons.

Geometry	Design Value
Trace Width (W1)	0.0115 in
Copper Weight (T1)	½ oz + Plating
Substrate thickness (H)	0.005 in
Construction	2116 56% RC
Panel Size	18 in x 24 in
Dk/Df	3.33/0.0018

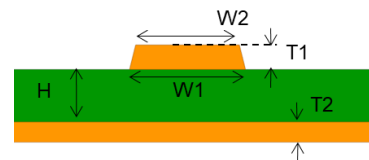


Figure 4 - Microstrip Transmission Line Design Parameters

To assess variations in loss, ten sets of microstrip coupons are prepared and tested for each type of copper and surface treatment. Each set consists of a 1-inch trace and 12.5-inch traces. Signal input is facilitated through two edge connectors located at both ends of the structure. Figure 5 displays a set of test coupons.



(a) 1-inch Coupon



(b) 12.5 inch Coupon

Figure 5 - Test Coupons

The scattering parameters are measured up to 70 GHz using a Vector Network Analyzer (VNA). Table 4 outlines the VNA test setup. A sample of the measured data is presented in Figure 6, which illustrates the insertion loss and impedance for ten sets of one specific copper type. The left plots depict the insertion loss for the 1-inch and 12.5-inch coupons, while the right plots show their corresponding impedances.

Table 4 - VNA Test Set-Up

VNA Make/Model	Anritsu / VectorStar
Frequency Start-Stop	10MHz-70GHz
Number of Frequency Points	7001
IF Bandwidth	1K Hz
Averaging type	Sweep-Sweep
Averaging Number	3
Connectors	End Launch 1.85mm (V) 67GHz
Measurement Cables	1.85mm V-Male 67GHz
Calibration	70GHz AutoCal

The Eigenvalue de-embedding method (refer to IPC-TM- 2.5.5.14 [1]) is employed to extract the loss per inch for each data set. Additionally, parameters such as effective dielectric constant and phase delay are also derived. This loss extraction method involves measuring the s-parameters of two microstrip transmission lines with differing lengths. Figure 7 presents an interval plot of the insertion loss at 28 GHz and 44 GHz.

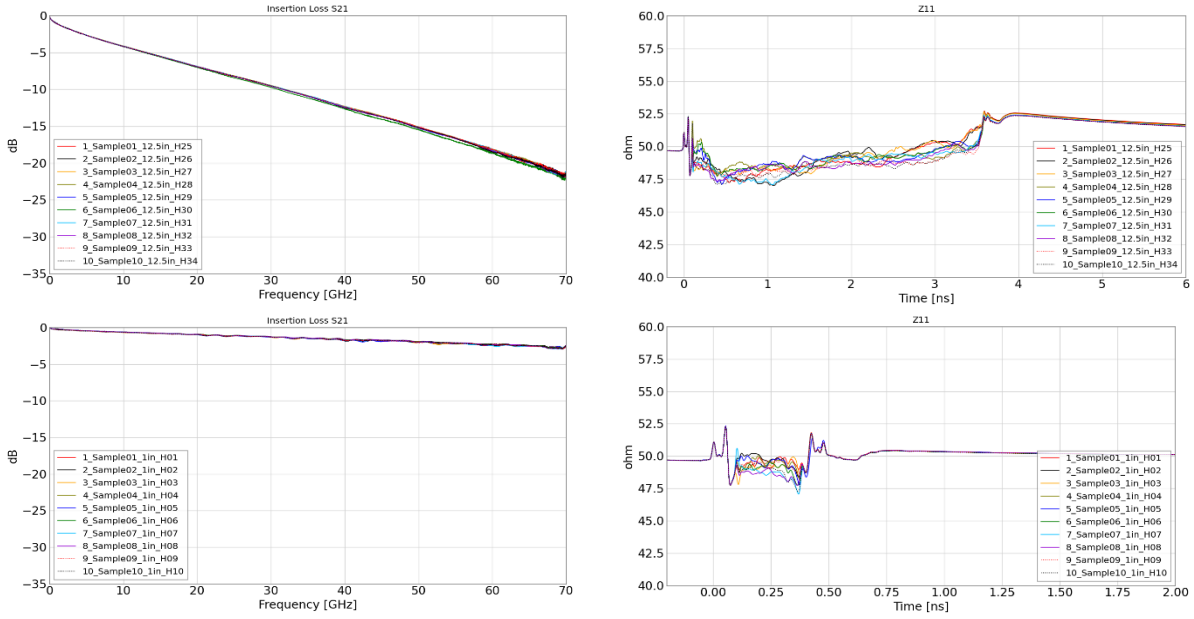


Figure 6 - Scattering Parameters

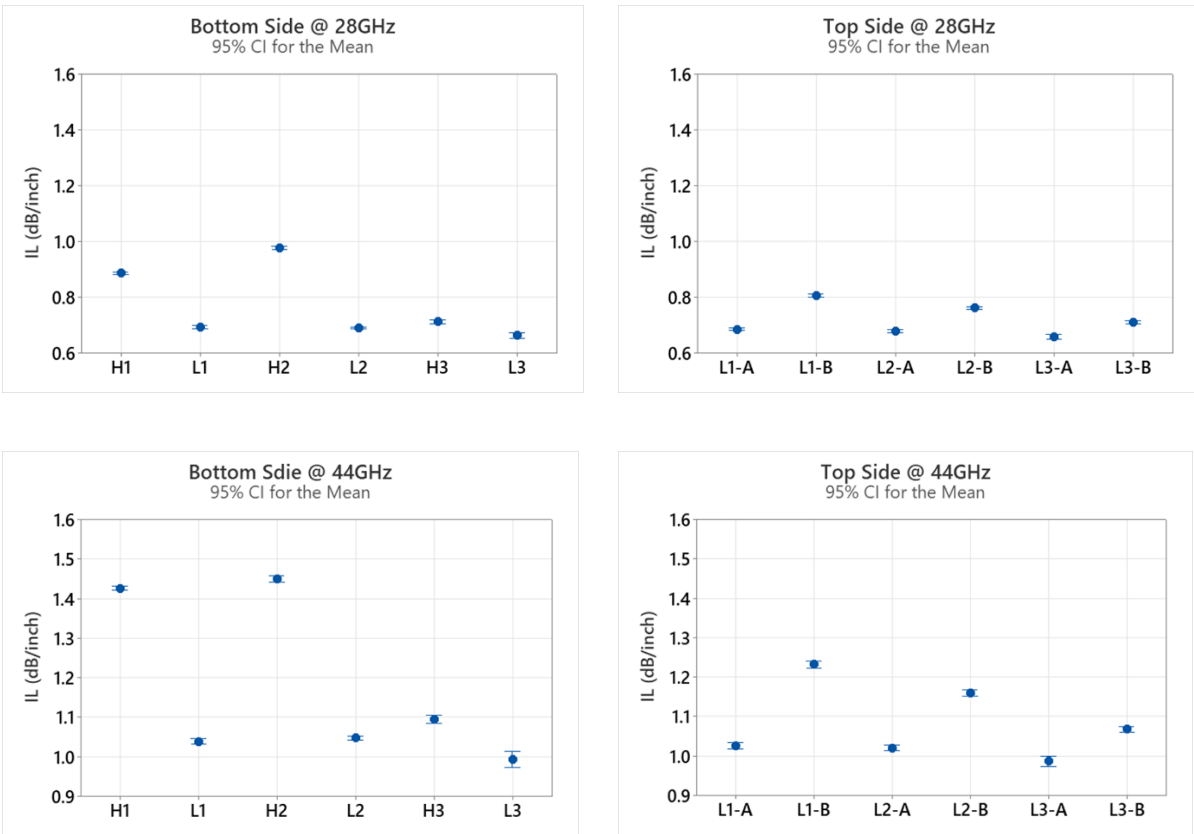


Figure 7 - Interval Plot of Extracted Insertion Loss (L=Low Profile, H=High Profile, A= OA1, B=OA2)

Surface Topology and Insertion Loss

Upon completion of the collection of scattering parameters, one sample from each group was cross-sectioned to verify the geometries of the fabricated samples and conduct correlation studies. Examples are shown in Figure 8.

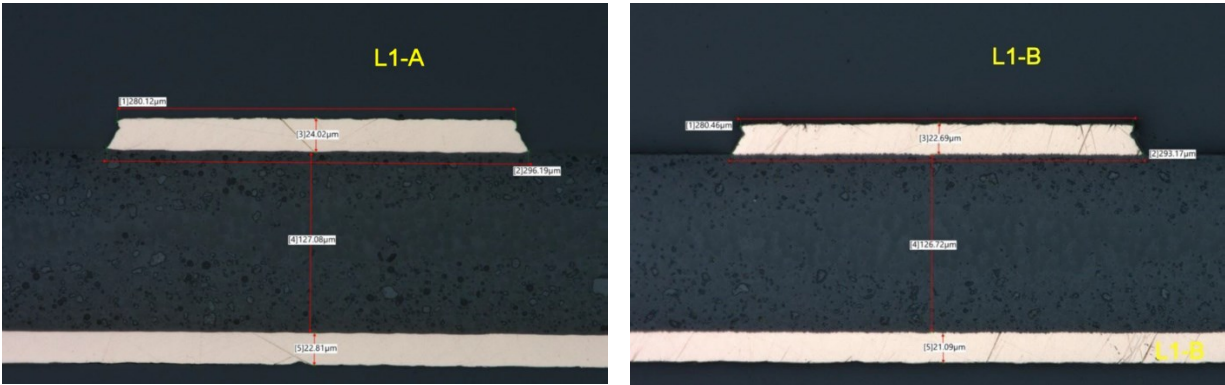


Figure 8 - Cross-Section Images

To further investigate the roughness profile, Scanning Electron Microscopy (SEM) was utilized to characterize the surface topology of the copper through cross-sectional analysis. Figure 9 presents the surface topology of the copper traces for several samples, revealing significant differences in tooth height, width, shape, and concentration.

The difference between the low-profile and high-profile traces is significant, as reflected in the surface topology measurements. In the low-profile trace, the dendrites are smaller, narrower, less condensed, and predominantly grow in a uniform direction. In contrast, the dendrites in the high-profile trace are longer, wider, denser, and exhibit a more random growth pattern. Additionally, the figure illustrates the impact of different oxide alternative (OA) types, specifically type A and type B. It is evident that type A results in a smoother surface compared to type B. Another important distinction is the formation of the dendrites. Although both the bottom side of the high-profile sample and the top side of the low-profile treated with type B oxide exhibit rough surfaces, the shape of the dendrites differs considerably.

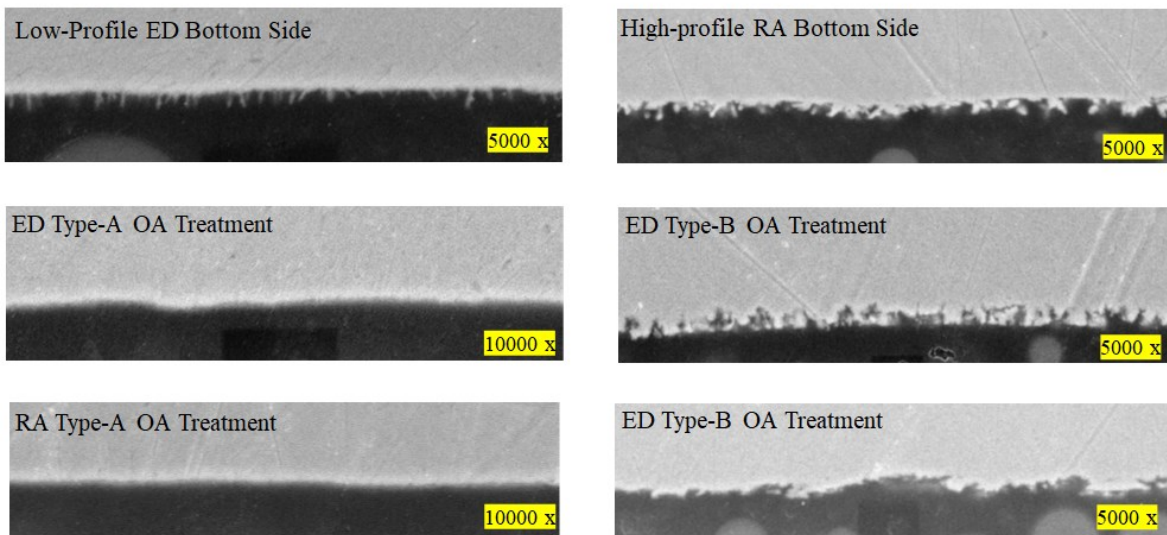


Figure 9 – SEMs of Various Surface Profiles

Non-Contact Profilometry

Surface roughness was measured on the foils before and after adhesion promotion treatment. 2x1” samples of each of the surface treatments were cut from the 18x24” foil sheet. The regions chosen for sampling were free of visual scratches, creases, and pigmentation. Five measurements were taken across the sample. Each measurement captured 0.06 mm², for a total measured area of 0.6 mm² per sample. A noncontact Keyence VK-X3000 laser microscope was chosen for measuring; the complimenting MultiFile Analyzer software was used for image processing. Per IPC 2.2.22, no filters were applied beyond a standard reference plane [2].

Though common in industry, surface roughness measurement techniques are not standardized and are often reported inconsistently in literature [3]. Some report the average absolute value in reference to the mean plane (Sa). Though informative, this measurement does not capture nor correlate to the surface area being measured. Another industry quantifier of surface roughness is Sq, or root mean square height. This calculation factors in the deviations from an average center line. Thus, this technique is better suited for applications investigating deviation from flatness, rather than a complete roughness profile. Another metric for reporting surface roughness is Sz, or the sum of the largest peak height and largest pit depth. This value does not factor in the topography of the entire measured area and only highlights two points, making it inadequate for this analysis. The Developed Interfacial Area Ratio (Sdr) was used to quantify surface roughness as it accounts for all geometries that increase surface area in comparison to a planar surface of the same dimensions (Eq. 1).

$$Sdr = \frac{\text{additional surface area}}{\text{planar xy area}} \quad \text{Eq. 1}$$

Results

A total of ten measurements were taken on each foil; the averages are reported in Table 5. Figure 10 is a chart of this data with 95% confidence intervals shown. Prior to adhesion promotion treatment, the Sdr of foil 1, 2, and 3 were 0.061, 0.11, and 0.053, respectively. Adhesion promotion chemistry “A” had a minimal impact on surface roughness with no statistical significance in foil 1 and 2, and a 0.047 increase in foil 3. Conversely, treatment “B” had a significant impact on surface roughness. It roughened foil 1, 2, and 3 by 0.539, 0.39, and 0.157, increasing their Sdr by 163%, 128%, and 119%, respectively. Between each brand of foil, 1 had the largest change in surface roughness between pre- and post-adhesion promotion chemistry “B”, followed by 2, then 3.

Table 5 - Summary of Sdr Results Pre- and Post-OA Treatments “A” and “B” reported with 95% Confidence Intervals. N=10, 5/sheet

Pre-Adhesion Promotion		Post-Adhesion Promotion	
Foil	Avg Sdr ± Std Dev	Foil-Treatment	Avg Sdr ± Std Dev
1	0.061 ± 0.004	1-A	0.06 ± 0.02
		1-B	0.6 ± 0.1
2	0.11 ± 0.03	2-A	0.09 ± 0.02
		2-B	0.5 ± 0.1
3	0.053 ± 0.003	3-A	0.10 ± 0.02
		3-B	0.21 ± 0.06

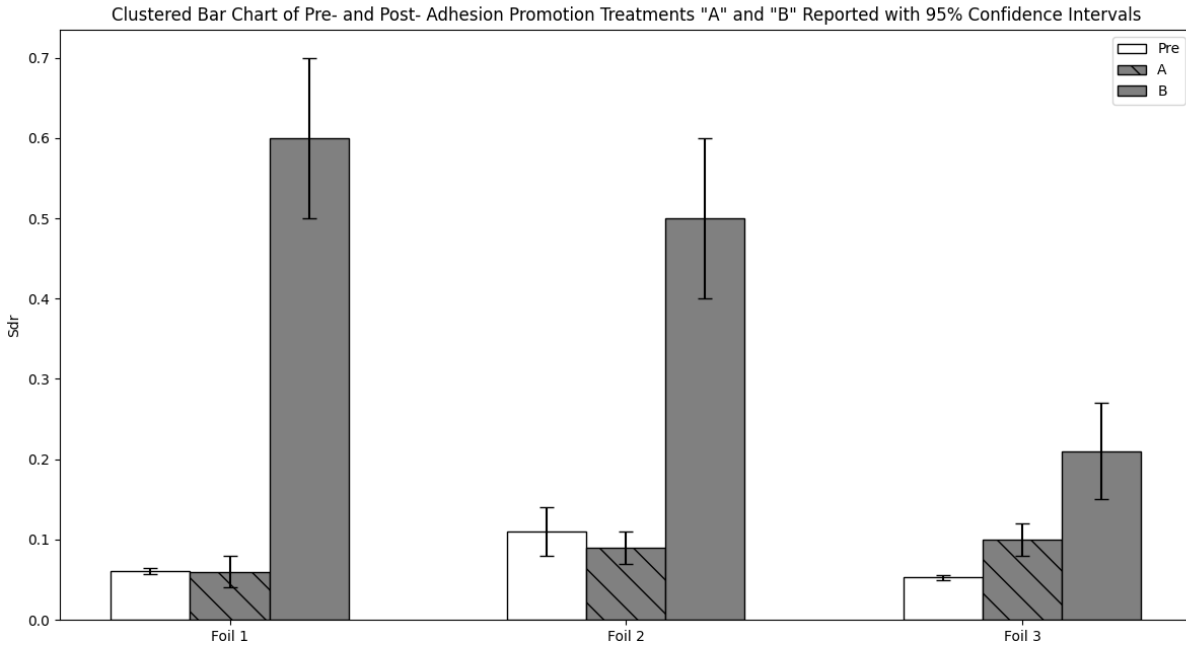


Figure 10 – Pre- and Post OA Treatment Roughness for the Three Copper Foil Grades

Resonance methods for individual materials

The characterization of conductive materials, particularly in high-frequency applications, demands precision and a deep understanding of how electromagnetic properties interact with conductive materials. A specialized measurement system using Ruby's dual-mode dielectric resonator (RuDR) and vector network analyzer (VNA), such as the Keysight Streamline P5008B used in this study, provides an efficient and reliable method for evaluating the properties of electrically thick conductive layers such as copper foils. The measurement system consists of a cylindrical RuDR, connected to a VNA through coaxial cables and a laptop as shown in Fig. 11.

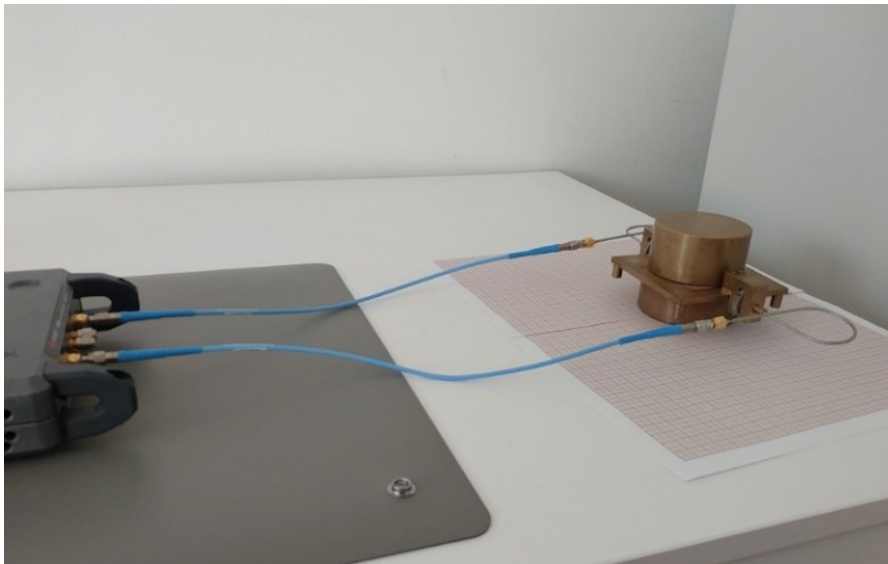


Figure 11 – Ruby Dielectric Resonator Test Set-Up

This ensures low-loss signal transmission and stable performance throughout the measurement process. A laptop, connected via USB to the VNA, provides real-time data acquisition and visualization, facilitating immediate analysis of the conductive samples. RuDR is a device specifically designed to focus on minimizing dielectric losses while precisely characterizing conductive layers. Operating in two different modes, TE011 and TE021, at frequencies around 13.8 GHz and 20.4 GHz, the RuDR enables dual-frequency measurements. This dual-mode operation not only extends the frequency spectrum but also increases the reliability of the extracted data, as results from both modes can be cross-referenced to ensure accuracy.

Foils are placed on top of the ruby resonator within a metallic cavity. Importantly, these conductive layers serve as the cavity's replaceable top and bottom walls, allowing direct contact with the resonator. This configuration ensures that the RuDR focuses on bulk material properties rather than surface-level anomalies, which is crucial when testing thick conductive materials. The RuDR is optimized for materials that satisfy the condition $h_s > 3\delta$, where h_s is the thickness of the conductive layer, and δ is the skin depth [4]. To ensure precision in measurement, the samples are pressed onto the resonator using calibrated weights to ensure even surface contact. This minimizes inconsistencies that could arise from improper placement and enhances the accuracy of the measurements.

Once the setup is complete, the VNA measures the resonant frequency and Q-factor of the resonator. The resonant frequency reflects how the electromagnetic fields distribute within the resonator, while the Q-factor indicates the level of energy dissipation. These two measurements are crucial for understanding the conductive properties of the sample. To extract material-specific data such as the effective conductivity (σ) and surface resistance (R_s), the resonant frequency and Q-factor are processed using dedicated software.

Last year, a set of measurements published at IPC APEX revealed a clear relationship between conductivity and surface roughness [5]. Building on these findings, the 5G Foil project was launched, focusing on the characterization of copper foils [6]. Initial results from this project have demonstrated a strong correlation between effective conductivity σ (measured at 13 GHz using the RuDR test fixture) and key surface roughness parameters: the Developed Interfacial Area Ratio, and the Maximum Height [7].

Conclusions

The experimental design for this project included the following parameters measured that showed several key interactions.

- 1) 3 copper vendors with 2 roughness levels on the matte side.
- 2) 3 surface treatment (OA) levels, High, Low and no Oxide.
- 3) 3 roughness parameters measured for each side of the foil. Sa, Sz and Sdr.
- 4) Conductivity measurements across 14-44GHz with 16 reported values each.
- 5) 4 loss values reported between 13-44 GHz.

The total number of measurements across all parameters was well over 5000. 28Ghz and 44Ghz loss and conductivity measurements were chosen to evaluate correlation between parameters.

Conductivity measurements correlate well with the roughness measured on the non-oxide alternative bottom side samples, in the 90% R^2 range. Higher roughness consistently showed lower conductivity. Conductivity measurements also correlate with loss measurements on the bottom side samples, above 90% R^2 .

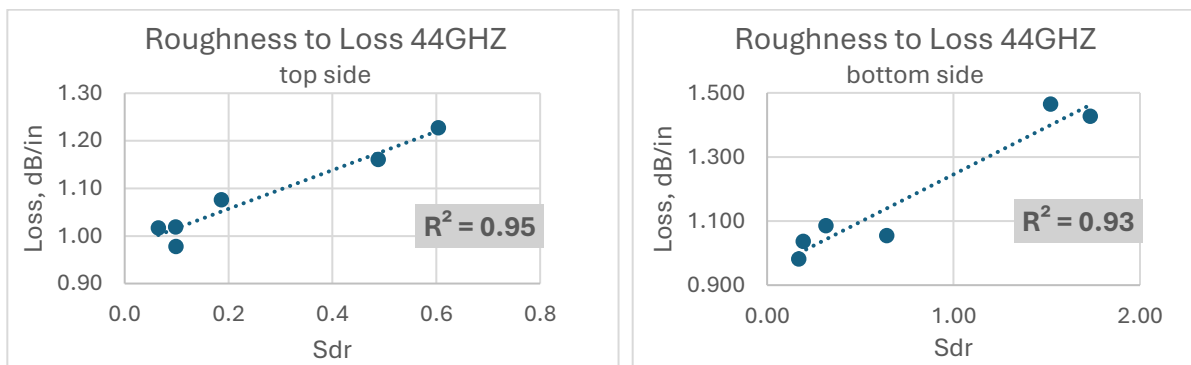


Figure 12 – Roughness vs loss correlation

Roughness measurements correlated well with loss measurements on both the top and the bottom side samples above 90% R^2 , as shown in figure 12. Highest roughness was on ED foil with the “B” alternative oxide treatment. This was true on both the bottom side and top side of the foil. Both surfaces of the RA foil were not as rough.

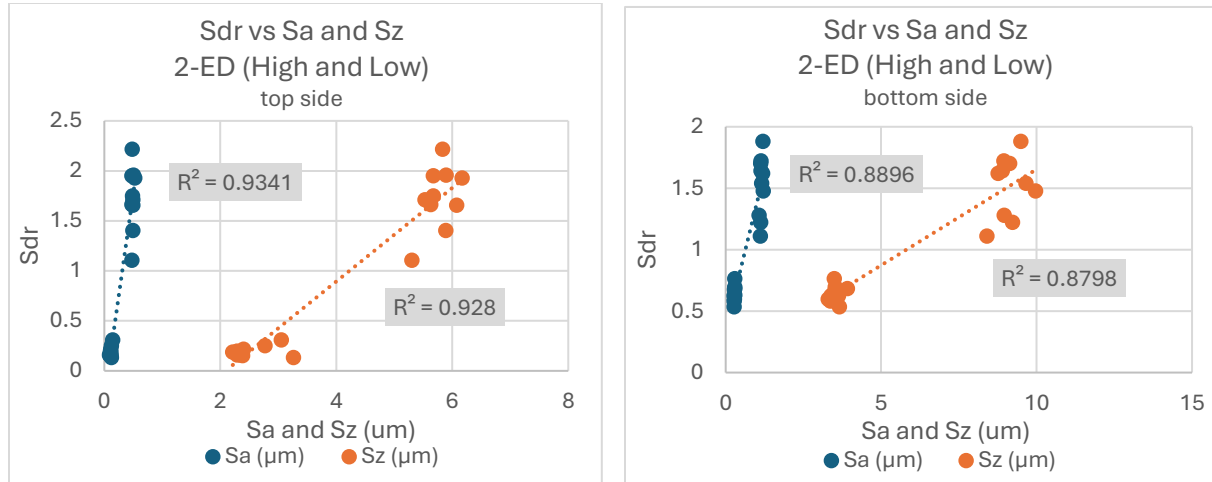


Figure 13 – Roughness measurement correlations

As shown in Figure 13, ED copper samples showed correlation above 90% R^2 for all roughness measurement types between, Sa vs Sz vs Sdr.

Variation of all measurements across the frequency ranges was consistent. R^2 values for those parameters within each copper type were well above 90%.

Because of the variables included in the design, some measurements had sample sizes of less than 5. Averages of each sample group were used to minimize the effect of sampling error. Only one outlier was found in the final correlation analysis.

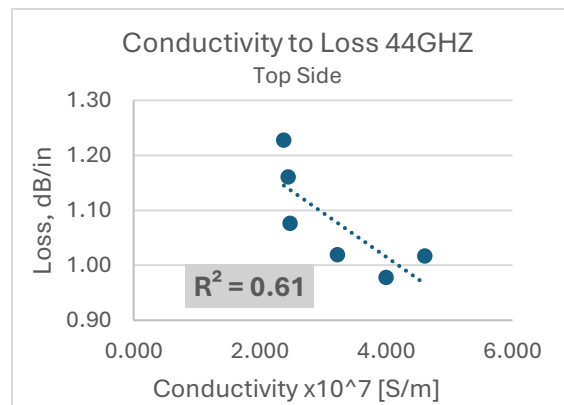


Figure 14 – Conductivity to Loss, top side down

Future work will need to be done to understand the conductivity correlations for OA-treated top side roughness and loss. These samples had measurably higher conductivity on the different oxide alternative treatments but did not show good correlation to the loss measurements as shown in Figure 14. Previous studies of conductivity and roughness indicated higher correlation than in this study. This is likely due to different copper types studied.

Reliability

As stated earlier, very low roughness copper foils are currently being used in commercial applications even though copper peel strengths with these foils fall below existing industry specifications. Reliability when using these foils has been validated through functional testing in multilayer PCBs, which is a time-consuming and costly process. As a result, modified or new test methods are being considered for testing CCL materials in order to expedite evaluations of new foil grades and to establish new quality and process control standards.

While the concern of delamination in multilayer PCBs is the most obvious risk from reduced copper peel strengths, whether this occurs at the copper foil to CCL dielectric interface or the oxide alternative treated side to the bonding dielectric, additional failure modes have been observed with these new extremely low-profile copper foils:

- Delamination at the etched CCL to prepreg bonding layer interface (Figure 15)
- Bond line CAF failure (Figure 16)

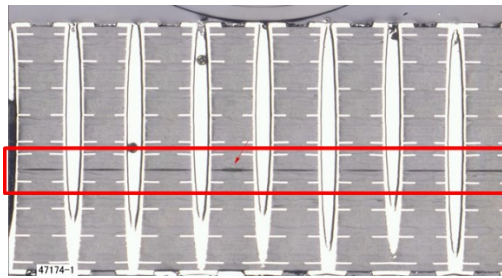


Figure 15 – Etched CCL Dielectric to Prepreg Dielectric Delamination

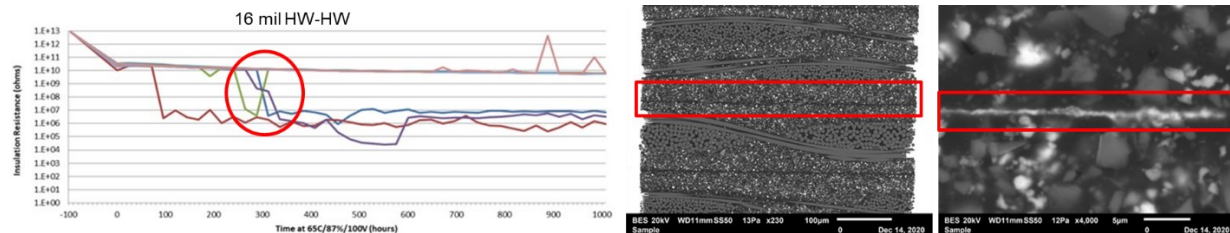


Figure 16 – CAF Failure at the Etched CCL to Prepreg Interface

Since there is much less surface area to provide mechanical bonding with these extremely low-profile foils, manufacturers use adhesion promotion chemicals to enhance adhesion of the copper foil to the polymers in the dielectric. These adhesion promoters must be compatible with the polymer used in the dielectric material. However, even poorly selected adhesion promoters may improve traditional measures of peel strength, but then fail in multilayer PCBs when thermally stressed or subjected to CAF testing where the PCBs are exposed to elevated temperatures, humidity and voltages for extended times.

To assess the capability of existing test methods to predict reliability of these foils and adhesion promoters, we selected an extremely low loss dielectric material and an extremely low-profile grade of copper foil. In one set of samples, we used an adhesion promoter known to be compatible with the dielectric, and in a second set of samples we chose an adhesion promoter not chemically compatible with the dielectric material. We then evaluated these samples using existing CCL test methods, as well as new or modified test methods thought to be more capable of assessing the bond reliability in these new foil and dielectric materials. Measurement variables for this initial

assessment are shown in Table 6. The glass transition temperature measurement was included simply to verify that the laminates were adequately cured.

Table 6 – Tests Performed on Laminate Samples

A	Glass Transition Temperature (check cure prior to testing other properties)
B	Peel Strength – As Is
C	Peel Strength – After thermal stress
D	Peel Strength – At elevated temperature
E	Peel Strength – After exposure to process solutions
F	Solder Float Time to Failure
G	Time to Delamination (copper clad sample) – 260, 288, 300C

Pressure cooker testing was also performed; however, the standard method uses laminates with copper removed and subjects them to 15 psi for 30 minutes. For this testing we etched copper peel strength coupons on the laminate and then measured peel strength values after the 30 minutes at 15 psi. Similarly, laminates with peel strength coupons were also subjected to temperature and humidity conditions of 85°C and 85% relative humidity for 50, 100 and 200 hours to determine if these conditions would degrade the bond strength between copper foil and dielectric. Table 7 lists the IPC test methods used for this evaluation, and Table 8 summarizes the test results.

Table 7 – IPC Test Methods Performed

	Testing Method	Sample type	Measurable	IPC TM-650 Test Method
1	Dynamic Mechanical Analysis (DMA)	Copper Clad Laminate	Glass Transition Temperature, Tg degrees C	2.4.24.2 [8]
2	Peel Strengths	Copper Clad Laminate	Peel Strength, lbs/in or N/mm	2.4.8C [9] 2.4.8.2 [10]
3	Solder Float to Failure	Copper Clad Laminate	Time to delamination, seconds	2.4.13F [11]
4	Thermomechanical Analysis (TMA) – Time to Delamination	Copper Clad Laminate	Time to delamination, minutes	2.4.24.1 [12] Method A

For peel strengths, the values in Table 8 are averages of four samples. Note that there is very little change in peel strength when an adhesion promoter known to be compatible with the dielectric material is used. In addition, solder float time to failure and time to delamination at 300°C are very good (T288 was not run on this sample given the T300 result). In contrast, when an adhesion promoter known not to be compatible is used, several of the test conditions led to decreases in peel strength, and solder float time to failure and time to delamination results are much lower compared to the samples with a known good adhesion promoter. Importantly, multilayer PCB testing with materials using this adhesion promoter did not result in delamination, but did exhibit bond line CAF failures. The decrease in peel strength with time spent at 85°C and 85% relative humidity may correlate with this phenomenon and should be investigated further.

It should be noted that while the non-compatible adhesion promoter exhibited a somewhat lower as received peel strength in this testing, in the authors' experience, other adhesion promoters that resulted in either bond line delamination or CAF failure sometimes exhibited quite good as-received peel strengths. So future work will focus on determining the best methods for assessment of extremely low loss laminate materials that use these new grades of copper foil.

Table 8 – Results Summary

Test		Extremely Low Loss Dielectric			
		Compatible Adhesion Promoter	% Change From As Received	Non-Compatible Adhesion Promoter	% Change From As Received
Peel Strength (lbs/in)	As Received	3.67	-	2.91	-
	After Thermal Stress	3.78	3.0%	2.91	0.0%
	After Process Solutions	3.58	-2.4%	2.50	-14.1%
	Elevated T - 125°C	3.58	-2.5%	2.42	-19.6%
	After Pressure Cooker (30 min @ 15psi)	3.68	0.3%	2.58	-13.6%
	50 hrs 85/85	3.59	-2.2%	2.48	-16.7%
	100 hrs 85/85	3.73	1.7%	2.25	-26.6%
	200 hrs 85/85	3.76	2.4%	2.19	-32.0%
Solder Float (sec)	Clad @ 550°F	1356		179	179
Tg, °C	DMA	202		199	199
Time to Delam (min)	T300	720+		3.3	3.3
	T288	Did not test		120	120

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Dell Technologies, Round Rock, TX, USA
Delton Technology Inc., Guangzhou, China
Denkai America, Camden, SC, USA
DuPont, Durham, NC, USA
Four Peaks Innovation, Scottsdale, AZ, USA
IBM, Rochester, MN, USA
Isola Group, Chandler, AZ, USA
MacDermid Alpha, Waterbury, CT, USA
QWED, Warsaw, Poland

References

- [1] *Measuring High Frequency Signal Loss and Propagation on Printed Boards with Frequency Domain Methods*, IPC-TM-650 2.5.5.14, IPC, Bannockburn, IL, USA, March 2021
- [2] *Noncontact Metallic Foil Surface Topography/Texture*, IPC TM-650 2.2.22, IPC, Bannockburn, IL, USA, May 2020
- [3] L. Toscano and E. Long, “Controlling Copper Roughness to Enhance Surface Finish Performance SMTAI 2015 Paper.” MacDermid, Waterbury, CT, USA

[4] J.Krupka, "Contactless methods of conductivity and sheet resistance measurement for semiconductors, conductors and superconductors", Meas. Sci. Technol. 24 (2013) 062001 DOI:10.1088/0957-0233/24/6/062001

[5] M. Celuch, M. Olszewska-Placha, L. Nowicki, P. Kopyt, J. Cuper, "Evaluation of Surface Roughness of Copper Foils for 5G Applications Using Novel mmWave Resonators", Apex Expo IPC, Anaheim, USA, 9th April, 2024. https://www.qwed.eu/ipc/156_Celuch_APEX%2024.pdf

[6] 5G_Foil project: https://qwed.eu/5g_foil.html

[7] M.Celuch, T. Devahif, T. Nalecz, and J. Rudnicki, "A Systematic Study of Correlation between Surface Roughness and Microwave Effective Conductivity of Copper Foils for Ultra-Low-Loss Applications", 25th International Microwave and Radar Conference (MIKON), pp. 314 – 315 Wroclaw, Poland DOI:10.23919/MIKON60251.2024.10633908

[8] *Glass Transition Temperature of Organic Films – DMA Method*, IPC TM-650 2.4.24.2, IPC, Bannockburn, IL, USA, July 1995

[9] *Peel Strength of Metallic Clad Laminates*, IPC TM-650 2.4.8C, IPC, Bannockburn, IL, USA, December 1994

[10] *Peel Strength of Metallic Clad Laminates at Elevated Temperature*, IPC TM-650 2.4.8.2, IPC, Bannockburn, IL, USA, December 1994

[11] *Solder Float Resistance Flexible Printed Wiring Materials*, IPC TM-650 2.4.13F, IPC, Bannockburn, IL, USA, May 1998

[12] *Time to Delamination (TMA Method) 12/94*, IPC TM-650 2.4.24.1, IPC, Bannockburn, IL, USA, December 1994